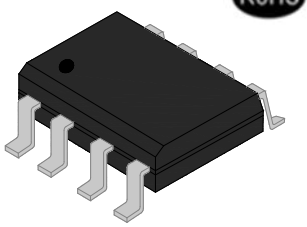
JIP83121D Dual Gate Uni-directional Overvoltage Protector

Rev.1.1

DESCRIPTION:



Package : SOP-8

JIP83121D is a dual-gate reverse-blocking unidirectional thyristor designed for the protection of dual-voltage ringing SLICs against overvoltages on the telephone line caused by lightning, a.c. power contact and induction.

The device chip is a four-layer NPNP silicon thyristor structure which has an electrode connection to every layer. For negative overvoltage protection the JIP83121D is used in a common anode configuration with the voltage to be limited applied to the cathode(K) terminal and the negative reference potential applied to the gate1(G1) terminal. For positive overvoltage protection the JIP83121D is used in a common cathode configuration with the voltage to be limited applied to the anode (A) terminal and the positive reference potential applied to the gate2 (G2) terminal.

The JIP83121D is a uni-directional protector and to prevent reverse bias, requires the use of a series diode between the protected line conductor and the protector. Further, the gate reference supply voltage requires an appropriately poled series diode to prevent the supply from being shorted when the JIP83121D crowbars.

Under low level power cross conditions the JIP83121D gate current will charge the gate reference supply. If the reference supply cannot absorb the charging current its potential will increase, possibly to damaging levels. To avoid excessive voltage levels a clamp diode may be added in shunt with the supply.

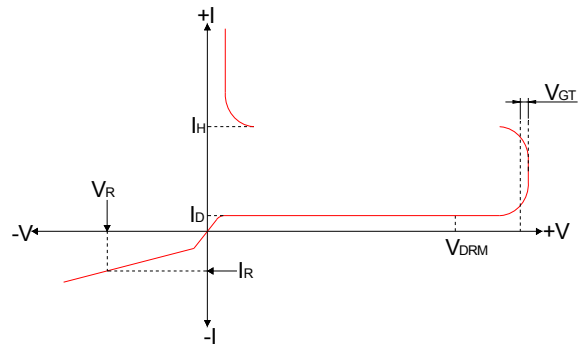
FEATURES:

- ✧ Overvoltage protection for dual-voltage ringing SLICs, programmable protection configurations up to ±100V.
- ✧ 5 lines protected by two JIP83121D and diode steering networks.
- ✧ Peak pulse current: I_{PP}=150A for 10/1000μs surge, 250A for 10/700μs surge, 500A for 8/20μs surge.
- ✧ Holding current: I_H=90mA min.
- ✧ Small outline surface mount package.
- ✧ Moisture sensitivity level: Level 3.
- ✧ IEC61000-4-2 (ESD) ±30kV (air), ±30kV (contact).

ELECTERICAL CAHRACTERISTIC

Symbol	Parameters
I_{DRM}	Repetitive peak off-state current
I_D	Off-state current
I_H	Holding current
V_{DRM}	Repetitive peak off-state voltage
V_R	Reverse voltage
I_R	Reverse current
I_{GT}	Gate trigger current
V_{GT}	Gate-cathode trigger voltage
C_{AK}	Anode-cathode off-state capacitance

V-I Curve



ABSOLUTE MAXIMUM RATINGS (T_A=25℃, RH=45%-75%, unless otherwise noted)

Parameter			Symbol	Value	Unit
Storage temperature range			T_{STG}	-40 to +150	℃
Junction temperature			T_J	-40 to +150	℃
Operating free-air temperature range			T_A	-40 to +85	℃
Non-repetitive peak on-state pulse current(Notes 1 and 2)					
10/1000μs	GR-1089-CORE, open-circuit voltage wave shape 10/1000μs)		I_{TSP}	150	A
5/310μs	(CCITT K.20/21 open-circuit voltage wave shape 7kV,10/700μs)			250	
8/20μs	(ANSI C62.41,open-circuit voltage wave shape 1.2/50μs)			500	
Non repetitive surge peak on-state current 50Hz,halfwave rectified sine wave(Notes 1 and 2)		0.1s	I_{TSM}	22	A
		1s		8	
		900s		3	

Note:

1. Initially the protector must be in thermal equilibrium with 0℃<T_J<70℃. The surge may be repeated after the device returns to its initial conditions. For operation at the rated current value, pins 1, 4, 5 and 8 must be connected together.
2. Above 70℃, derate linearly to zero at 150℃ lead temperature.

ELECTRICAL CHARACTERISTICS (T_A=25℃)

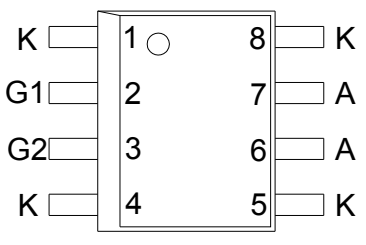
Symbol	Parameter	Test conditions		Value			Unit
				Min.	Typ.	Max.	
I_D	Off-state current	V_d=70V, I_G=0		-	-	1	μA
I_{DRM}	Repetitive peak off-state current	V_d=V_{DRM}=100V, I_G=0, 0℃~70℃		-	-	10	μA
I_H	Holding current	I_T=1A, di/dt=-1A/ms	T_J=0~70℃	-	-	300	mA
			T_J=25℃	90	-	-	
			T_J=70℃	60	-	-	
I_R	Reverse current	V_R=0.3V		-	-	1	mA
I_{G1T}	Gate G1 trigger current	I_T=+1A, $t_{p(g)}$=20μs		-	-	+200	mA
I_{G2T}	Gate G2 trigger current	I_T=+1A, $t_{p(g)}$=20μs		-	-	-180	mA
V_{G1T}	G1-K trigger voltage	I_T=+1A, $t_{p(g)}$=20μs		-	-	+1.8	V
V_{G2T}	G2-A trigger voltage	I_T=+1A, $t_{p(g)}$=20μs		-	-	-1.8	V
C_{AK}	Anode-cathode off-state capacitance	f=1MHz,V_d=1V_{rms},I_G=0, V_D=5V(Note 3)		-	-	100	pF

Note:3 These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The unmeasured device terminals are a.c. connected to the guard terminal of the bridge.

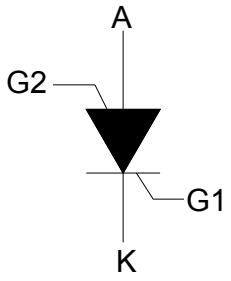
THERMAL CHARACTERISTICS (T_A=25℃)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
$R_{\theta JA}$	Thermal resistance junction to ambient	T_A=25℃	-	-	105	℃/W

SOP PACKAGE TOP VIEW AND DEVICE SYMBOL

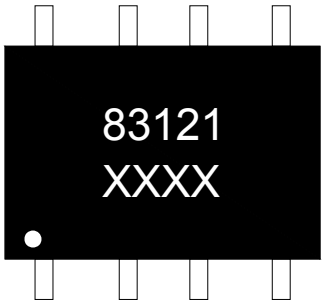


Package (Top view)



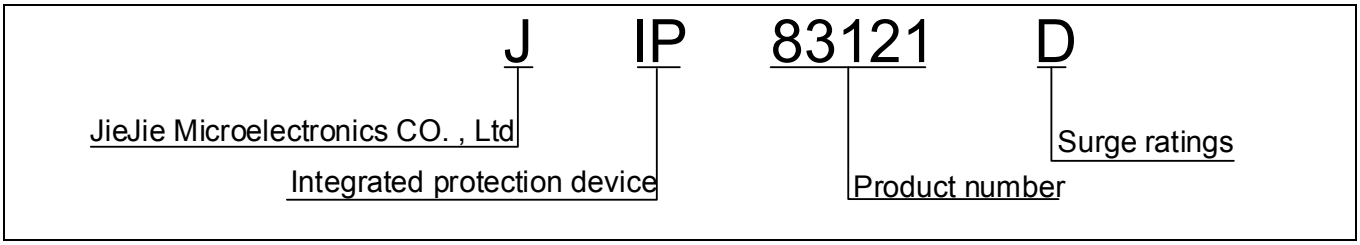
Device symbol

MARKING



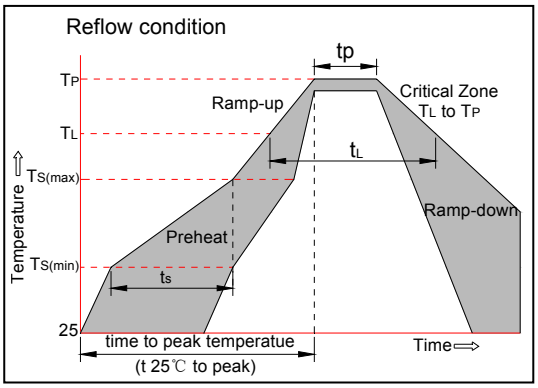
83121：Device marking code
XXXX：Date of manufacture

ORDERING INFORMATION



SOLDERING PARAMETERS

Reflow Condition		Pb-Free assembly (see figure at right)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150℃
	-Temperature Max($T_{s(max)}$)	+200℃
	-Time (Min to Max) (ts)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L)to peak)		3℃/sec. Max
$T_{s(max)}$ to T_L - Ramp-up Rate		3℃/sec. Max
Reflow	-Temperature(T_L)(Liquidus)	+217℃
	-Temperature(t_L)	60-150 secs.
Peak Temp (T_p)		+260(+0/-5)℃
Time within 5℃of actual Peak Temp (t_p)		30secs.Max
Ramp-down Rate		6℃/sec. Max
Time 25℃ to Peak Temp (T_P)		8 min. Max
Do not exceed		+260℃



APPLICATION INFORMATION

Multiple line overvoltage protection (Fig.1)

Fig.1 shows two JIP83121D devices protecting many lines. Line conductor positive overvoltage protection is given by the steering diode array connected to the anode of the upper JIP83121D and the JIP83121D itself. The JIP83121D gate reference voltage is the positive battery supply, $+V_{BAT}$. The initial limiting voltage will be the sum of the voltages of the battery, the forward biased conductor diode, the gate trigger of the JIP83121D and the forward biased reference voltage blocking diode. Typically, the conductor voltage will be initially limited at 2.5V above the $+V_{BAT}$ value.

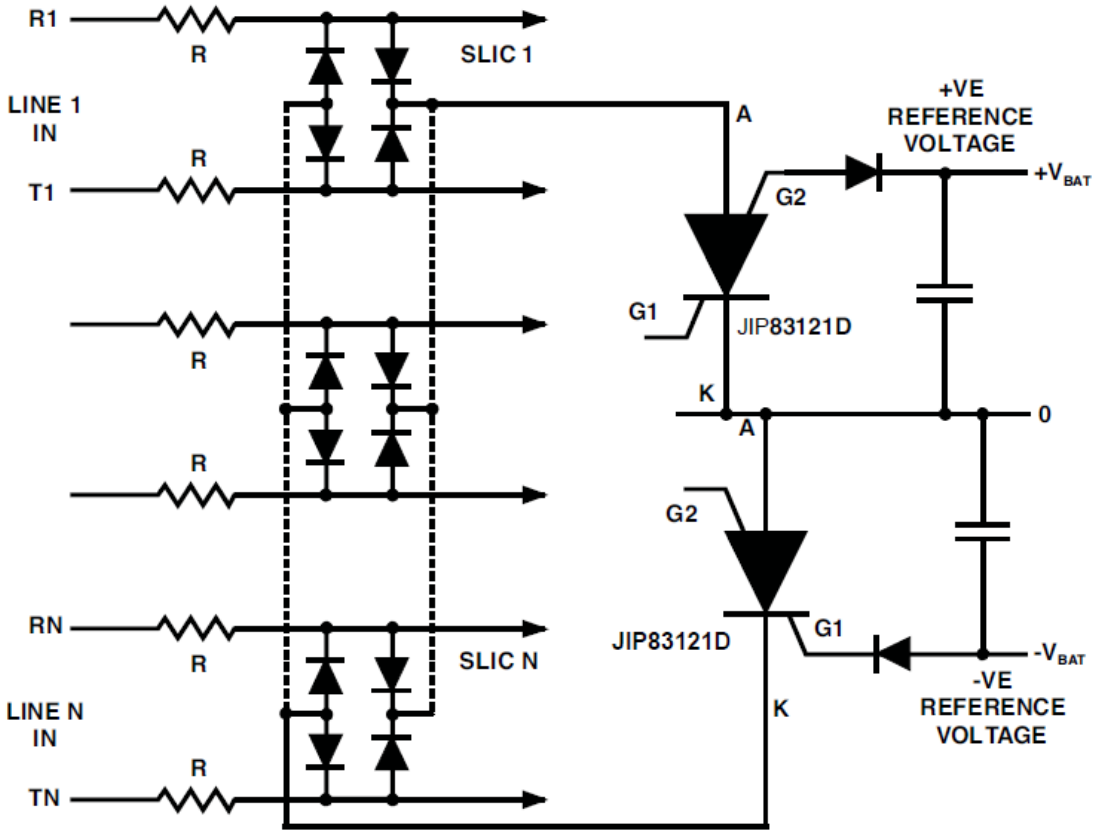


Fig.1. N line positive and negative overvoltage protection

Line conductor negative overvoltage protection is given by the diode steering array connected to the cathode of the lower JIP83121D and the JIP83121D itself. The T JIP83121D gate reference voltage is the negative battery supply, $-V_{BAT}$. The initial limiting voltage will be the sum of the voltages of the battery, the forward biased conductor diode, the gate trigger of the JIP83121D and the forward biased reference voltage blocking diode. Typically the conductor voltage will be initially limited at 2.5V below the $-V_{BAT}$ value.

When a JIP83121D crowbars and grounds all conductors of the appropriate polarity, the device current will be the sum of all the SLIC output currents. This will usually exceed the JIP83121D holding current. To switch off the JIP83121D and restore normal operation, the grounded condition of the SLIC output must be detected and the SLIC outputs turned off.

The 150A rating of the JIP83121D allows a large number of lines to be protected against currents caused by lightning. For example, if a recommendation K.20 10/700 generator was connected to all lines, together with 350V primary protection and a series conductor resistance (R) of 25Ω, the maximum conductor current before the primary protection operated would be 350/25=14A or 28A per line. For a total return current of about 150 A the number of lines would be 150/28=5. At this current level, 5x28=140A, the generator voltage would be 140 x ((25+25)/ 10+15) = 2800V. Another limitation is long term power cross. The long term power cross capability of the JIP83121D is 3A peak or 2.1A rms. If the line conductor overcurrent protection was given by a PTC thermistor which tripped at 0.2A, the maximum number of the conductors becomes 2.1/0.2 = 10 or 5 lines.

Battery supply impedance (Fig.2)

In many designs, the battery supply voltages are generated by switching mode power supplies. This type of power supply cannot be charged like a battery. Feeding a charging current to a switching mode power supply will usually cause the supply to stop switching and the voltage to rise. The gate current of the JIP83121D is a charging current for the supply. To avoid the supply voltage from rising and damaging the connected SLICs, an avalanche diode voltage clamp can be connected across the supply . Fig.2.(A).

Another approach is to reduce the gate charging current for the supply by a transistor buffer Fig.2.(B). If the transistor gain was 50, a 200mA gate current would be reduced to a supply charging current of 200/50=4mA. In both cases, the dissipation in the control devices can be substantial and power capability needs to be taken into account in device selection.

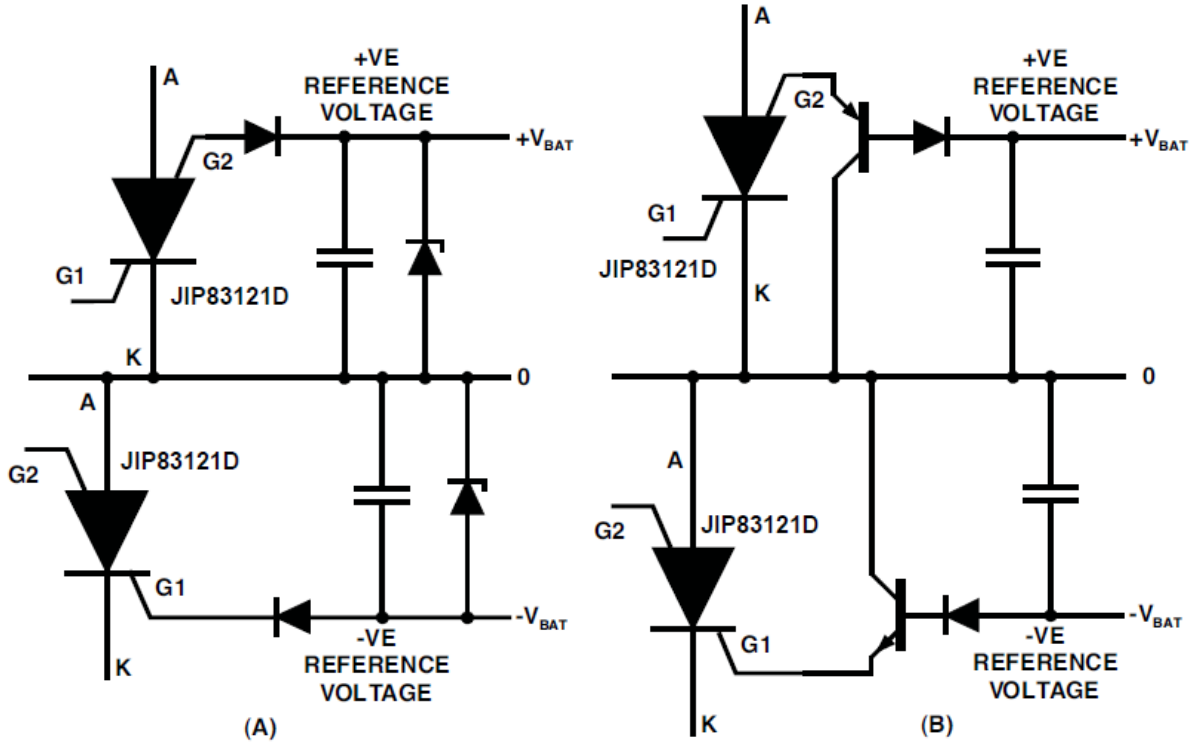
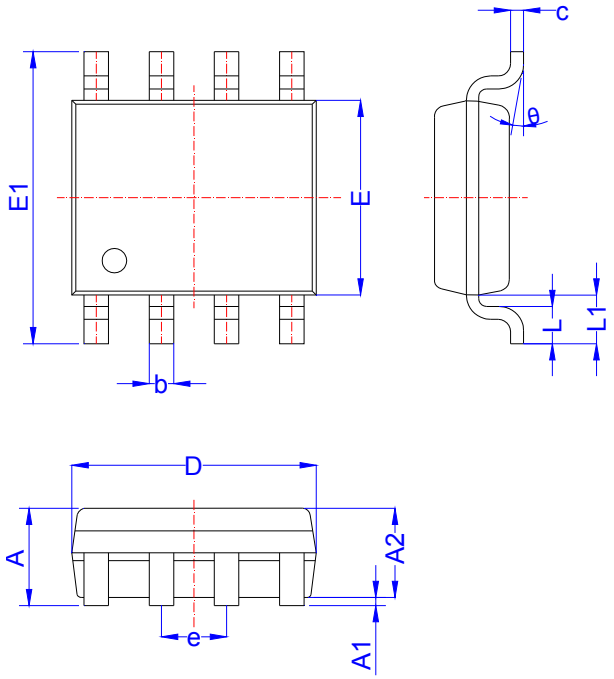


Fig.2. reference voltage control by (A) breakdown diodes or (B) by transistor buffers

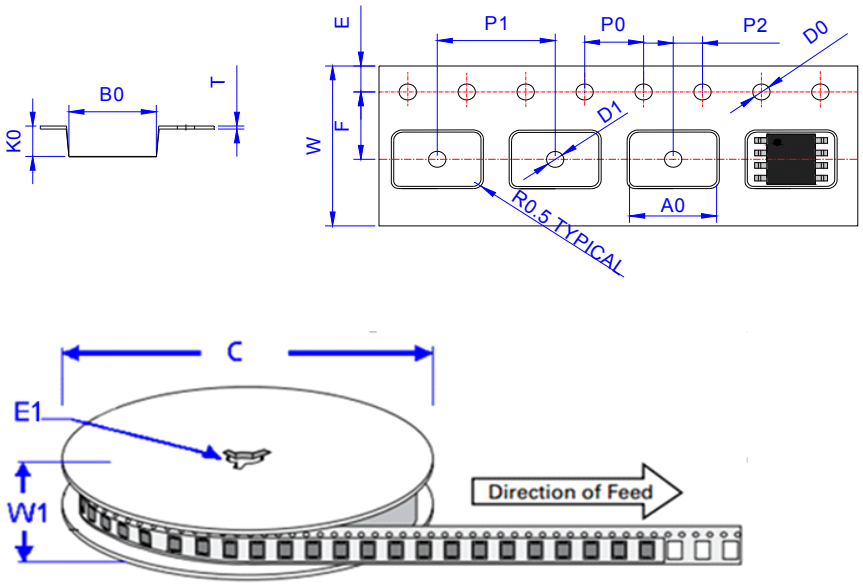
PACKAGE MECHANICAL DATA



SOP-8

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.70	0.053		0.067
A1	0.04		0.18	0.002		0.007
A2	1.30		1.55	0.051		0.061
b	0.31		0.51	0.012		0.020
c	0.17		0.25	0.007		0.010
D	4.65		5.10	0.183		0.201
E	3.70		4.10	0.146		0.161
E1	5.80		6.20	0.228		0.244
e	1.14	1.27	1.40	0.045	0.050	0.055
L	0.40		0.77	0.016		0.030
L1	0.825		1.225	0.032		0.048
θ	0°		8°	0°		8°

TAPE AND REEL SPECIFICATION-SOP-8



Ref.	Dimensions	
	Millimeters	Inches
A0	6.6±0.10	0.260 ± 0.004
B0	5.3±0.10	0.209 ± 0.004
C	330	13.0
D0	1.50±0.10	0.059 + 0.004
D1	1.50±0.10	0.059 + 0.004
E1	13.3±0.3	0.524± 0.012
E	1.75±0.1	0.069± 0.004
F	5.5±0.05	0.217 ± 0.002
K0	2.1±0.1	0.083 ± 0.004
P0	4.0±0.1	0.157± 0.004
P1	8.0±0.1	0.315± 0.004
P2	2.0±0.05	0.079 ± 0.002
T	0.24±0.1	0.009 ± 0.002
W	12.0±0.3	0.472 ± 0.012
W1	15.7±2.0	0.618 ± 0.079

PART No.	UNIT WEIGHT (g/PCS) typ.	REEL (PCS)	PER CARTON (PCS)	DESCRIPTION
JIP83121D	0.077	4,000	64,000	13 inch reel pack

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